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1765

PATENT

Attorney Reference Number 6319-56134

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chin-Huang Chang

Art Unit: 1765

Application No.: 09/660,753

Filed: September 13, 2000

For: METHOD FOR REDUCING SIZE OF SEMICONDUCTOR UNIT IN PACKAGING PROCESS

Examiner: Lan Vinh

Date: March 17, 2003

CERTIFICATE OF MAILING

I hereby certify that this paper and the documents referred to as being attached or enclosed herewith are being deposited with the United States Postal Service on March 17, 2003 as First Class Mail in an envelope addressed to: BOX NON-FEE AMENDMENT, COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

Stacey C. Slater
Attorney for Applicant

TRANSMITTAL LETTER

BOX NON-FEE AMENDMENT
COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

Enclosed is an Amendment and Response to Office Action for the above application. The fee has been calculated as shown below.

CLAIMS AS AMENDED						
For	No. after amendment	No. paid for previously		Present Extra	Rate	Fee
Total Claims	20	- 20*	=	0	$9.00	$ 0.00
Indep. Claims	3	- 3**	=	0	$42.00	$ 0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						$0.00

* greater of twenty or number for which fee has been paid.
** greater of three or number for which fee has been paid.

☒ No additional fee should be required to file this Amendment and Response to Office Action.

☒ Please charge any fee that the Patent Office believes may be required in connection with filing this Amendment and Response to Office Action and any extension of time to Deposit Account No. 02-4550. A copy of this sheet is enclosed.

☒ Please return the enclosed postcard to confirm that the items listed above have been received.

Respectfully submitted,

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Stacey C. Slater
Attorney for Applicant

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AMENDMENT AND RESPONSE TO OFFICE ACTION

This responds to the Office Action dated Dec 17, 2002, concerning the application referenced above. Please amend the application as follows.

5,532,189.

Please cancel claims 1-20 without prejudice.

21. (New) A method for reducing the size of at least a semiconductor unit in a process of making a package including a carrier and said semiconductor unit, said semiconductor unit including a first surface and a second surface, said second surface having no electrical connection device thereon, said method comprising:

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attaching at least a part of said first surface to said carrier according to a configuration of lead-on-chip packaging; and

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etching said semiconductor unit from said second surface to reduce the thickness of said semiconductor unit until the thickness of said semiconductor unit meets an expected specification.

5658,557

22. (New) The method according to claim 21 wherein said semiconductor unit is etched by using beams of light.

6 184,060

21, 24-26, 28-31, 32-38
22, 23, 32
27, 33, 39, 40

23. (New) The method according to claim 21 wherein said semiconductor unit is etched by using plasma.

24. (New) The method according to claim 21 wherein said expected specification means that the thickness of said semiconductor unit measured relative to said first surface is within a specified range.

25. (New) The method according to claim 21 wherein said semiconductor unit is a wire bonding chip.

26. (New) The method according to claim 21 wherein etching comprises a step of shielding at least a part of said semiconductor unit and said carrier to prevent the quality of said semiconductor unit and said carrier from being affected.

27. (New) The method according to claim 21 further comprising, before attaching, grinding said semiconductor unit until the size thereof approximates said expected specification.

28. (New) The method according to claim 21 wherein etching comprises a step of using a fixture to shield at least a part of said semiconductor unit and said carrier for preventing the quality of said semiconductor unit and said carrier from being affected.

29. (New) The method according to claim 21 wherein said semiconductor unit is a wire bonding chip and is partly attached to said carrier via adhesive material.

30. (New) The method according to claim 21 wherein said carrier is a chip carrier, said semiconductor unit includes at least an electrical connection device located on said first surface, and attaching includes connecting said electrical connection device to said chip carrier.

31. (New) A method for reducing the size of at least a semiconductor unit in a process of lead-on-chip packaging wherein said semiconductor unit includes a first surface and a second surface, said first surface having at least an electrical connection device thereon, said second surface having no electrical connection device thereon, said method comprising:

attaching said semiconductor unit to a chip carrier in such a way that said semiconductor unit and said chip carrier are in a configuration of lead-on-chip, with said first surface facing said chip carrier and said second surface exposed; and

etching said semiconductor unit from said second surface to reduce the thickness of said semiconductor unit until the thickness of said semiconductor unit meets an expected specification.

32. (New) The method according to claim 31 wherein etching includes applying beams of light on said second surface.

33. (New) The method according to claim 31 further comprising, before attaching, grinding said semiconductor unit until the size of said semiconductor unit approximates said expected specification.

34. (New) The method according to claim 31 wherein said expected specification means that the thickness of said semiconductor unit measured relative to said first surface is within a specified range.

35. (New) The method according to claim 31 wherein said configuration of lead-on-chip means that part of said first surface is connectible with said chip carrier via adhesive material and said semiconductor unit is electrically connectible with said chip carrier via said electrical connection device.

36. (New) The method according to claim 31 wherein attaching includes a step of connecting at least part of said first surface to said chip carrier via adhesive material.

37. (New) The method according to claim 31 wherein etching comprises shielding at least part of said semiconductor unit and said carrier to prevent the quality of said semiconductor unit and said carrier from being affected.

38. (New) The method according to claim 31 further comprising electrically connecting said semiconductor unit to said chip carrier via said electrical connection device after etching.

39. (New) A method for reducing the size of at least a semiconductor unit in a process of packaging said semiconductor unit wherein said semiconductor unit includes a first surface and a second surface, said second surface having no electrical connection device thereon, said method comprising:

attaching at least a part of said first surface to said carrier;

using a fixture to surround said carrier and said semiconductor unit while expose said second surface; and

etching said semiconductor unit from said second surface to reduce the thickness of said semiconductor unit until the thickness of said semiconductor unit meets an expected specification.

40. (New) The method according to claim 39 wherein said carrier and said semiconductor unit are surrounded in such a way that said carrier and said semiconductor unit are shielded from etching except said second surface.

REMARKS

1. Applicant appreciates the Examiner's thorough review of the present application, and respectfully requests reconsideration in light of the foregoing amendments and the following remarks.

2. Applicant appreciates the Examiner's indications that: (1) claim 11 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112; (2) claims 12-18 are objected to as being dependent on a rejected claim but would be allowable to overcome the rejection(s) under 35 U.S.C. 112 and to include all the limitations of base claim and/or intervening claims; and (3) claim 9 would be allowable if rewritten in independent form including all the limitations of base claim and/or intervening claims.

3. Accordingly, applicant has added: new independent claim 21 to overcome the rejection(s) under 35 U.S.C. 112 and to include the subject matter contained in claim 1 (filed on Oct 03, 2002) and claim 9 (filed on Oct 03, 2002); new claims 22-30 to depend on new independent claim 21; new independent claim 31 to overcome the rejection(s) under 35 U.S.C. 112; new claims 32-38 to depend on new independent claim 31; new independent claim 39 to include the subject matter contained in claim 1 (filed on Oct 03, 2002) and original claim 8; and new claim 40 to depend on new independent claim 39.

4. New claims 22-30 ultimately depend on new independent claim 21, and new claims 32-38 ultimately depend on new independent claim 31, and these claims therefore are